

Bioelectronics and Neuromorphic Computing with Organic Electrochemical Transistors – 4th Lecture

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4. Processing of Organic Electrochemical Devices

4.4 Scaling of OECTs

- **Which device properties are influenced by scaling**
 - Threshold voltage, cut-off frequency, transconductance, on/off ratio, short channel properties, parasitic capacitance, operation voltage
- **Which device parameters can scaled**
 - W/L, thickness of OMIEC, conductivity and thickness of electrolyte, gate area, S/D overlap

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4.4 Scaling of OECTs

- **Scaling of electronic circuit**
 - Electronic circuit is described by a voltage controlled (V_{GS}) resistor \rightarrow transconductance scales linear with V_{GS} , channel cross-section, mobility and capacitance
 - Main assumptions
 - C^* does not depend on thickness! Demonstrator for devices from 2.7nm to 5 μ m thickness
 - Mobility does not depend on gate voltage (very rough assumption but probably true due to high charge concentration)
 - No contact resistance

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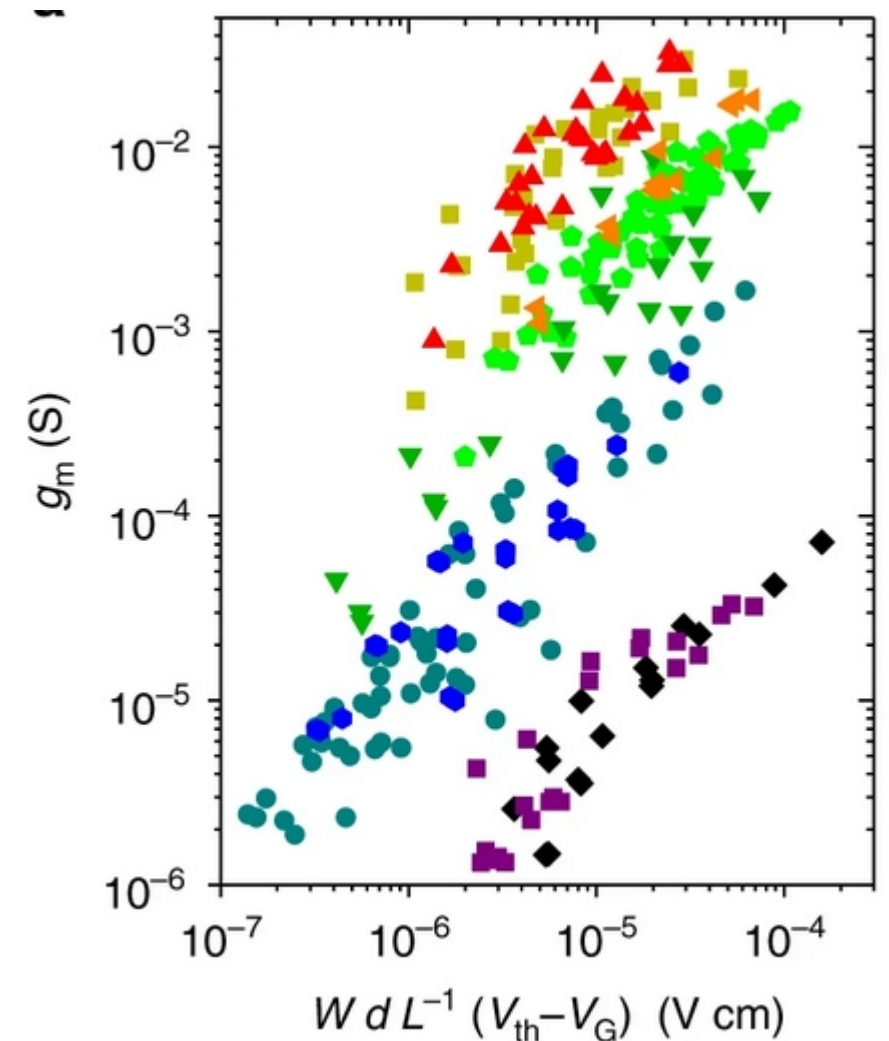
4.4 Scaling of OECTs

- **Scaling of electronic circuit**

- Transconductance scales according to

$$g_m = \frac{Wd}{L} \mu C^* (V_{th} - V_G)$$

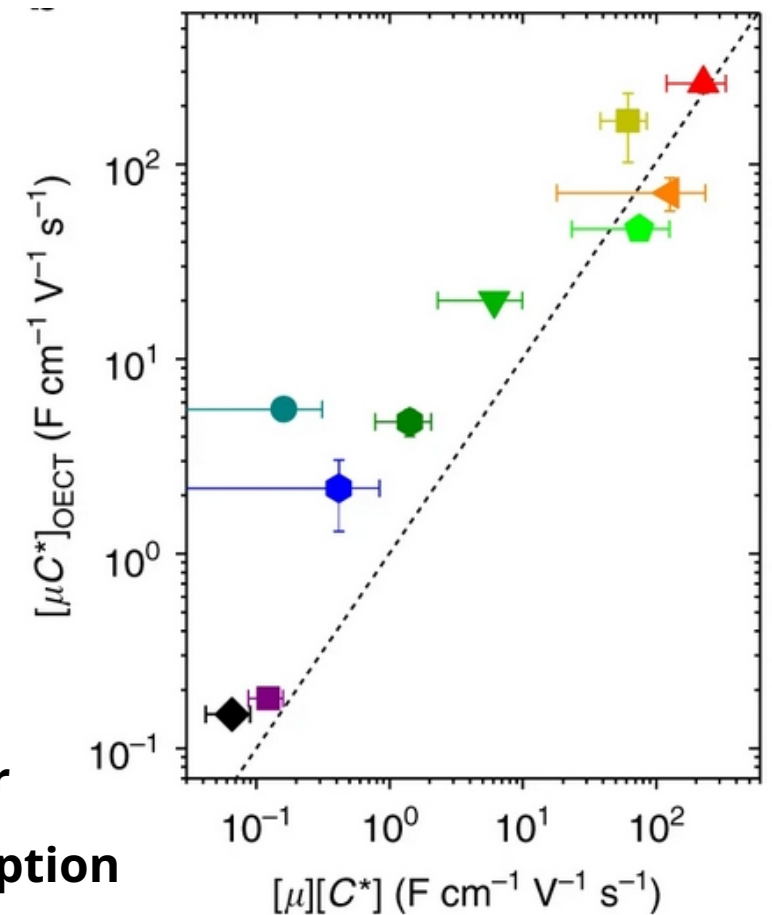
- Scaling has been demonstrated for L from $<1\mu\text{m}$ to mm and W from μm to mm
- Materials mainly differ in their μC^* product!



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4.4 Scaling of OECTs

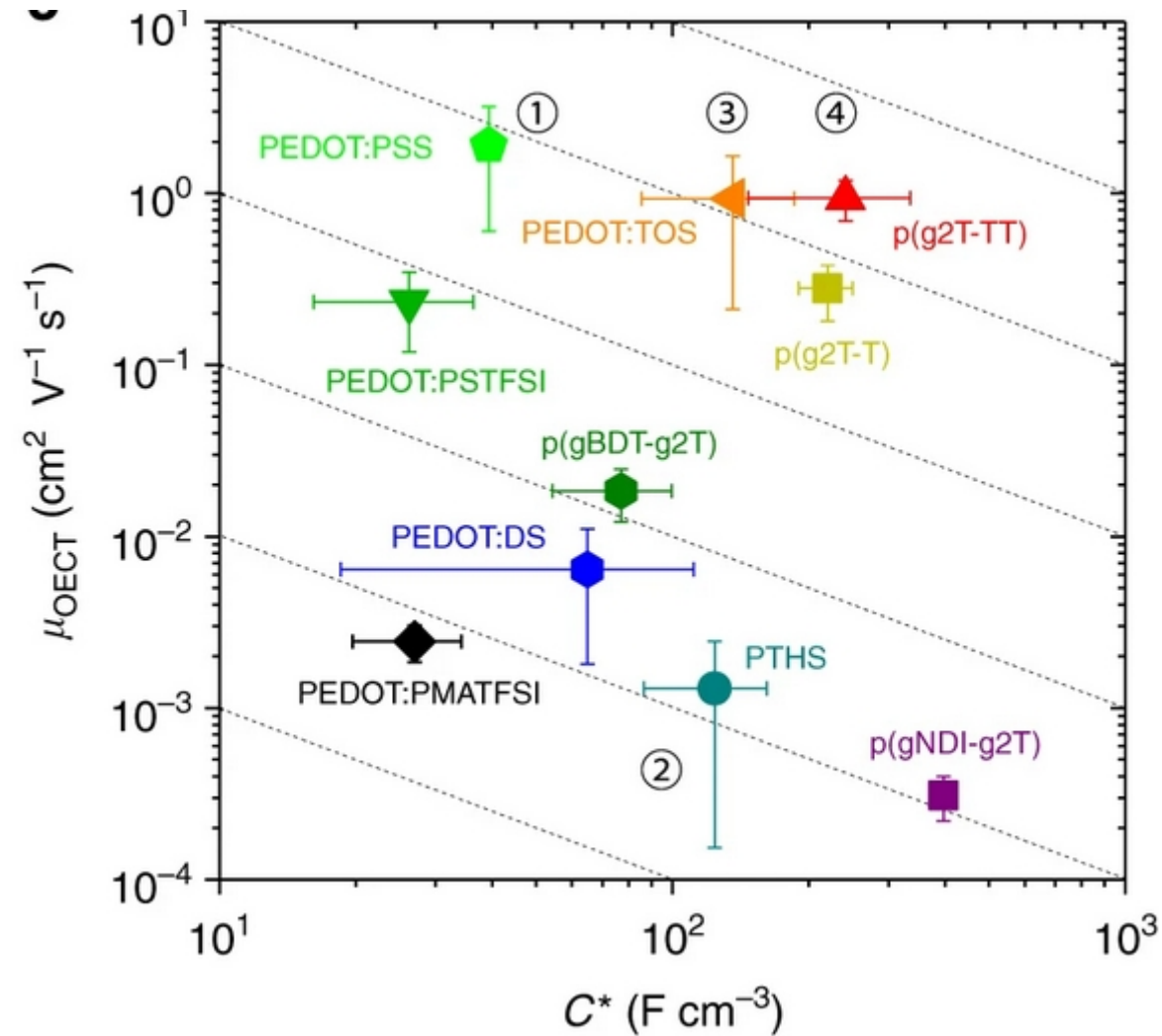
- μC^* Product
- μC^* Product from g_m analysis has been used a main material benchmark
- μ and C^* can be determined independently (but difficult) and confirm the g_m method to determine μC^*
- High μC^* is favorable for sensing \rightarrow differently translates into transistor gain!
- **However, μC^* can be very misleading looking into transistor switching (μ could be low but C^* high \rightarrow high power consumption but slow devices)**



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4.4 Scaling of OECTs

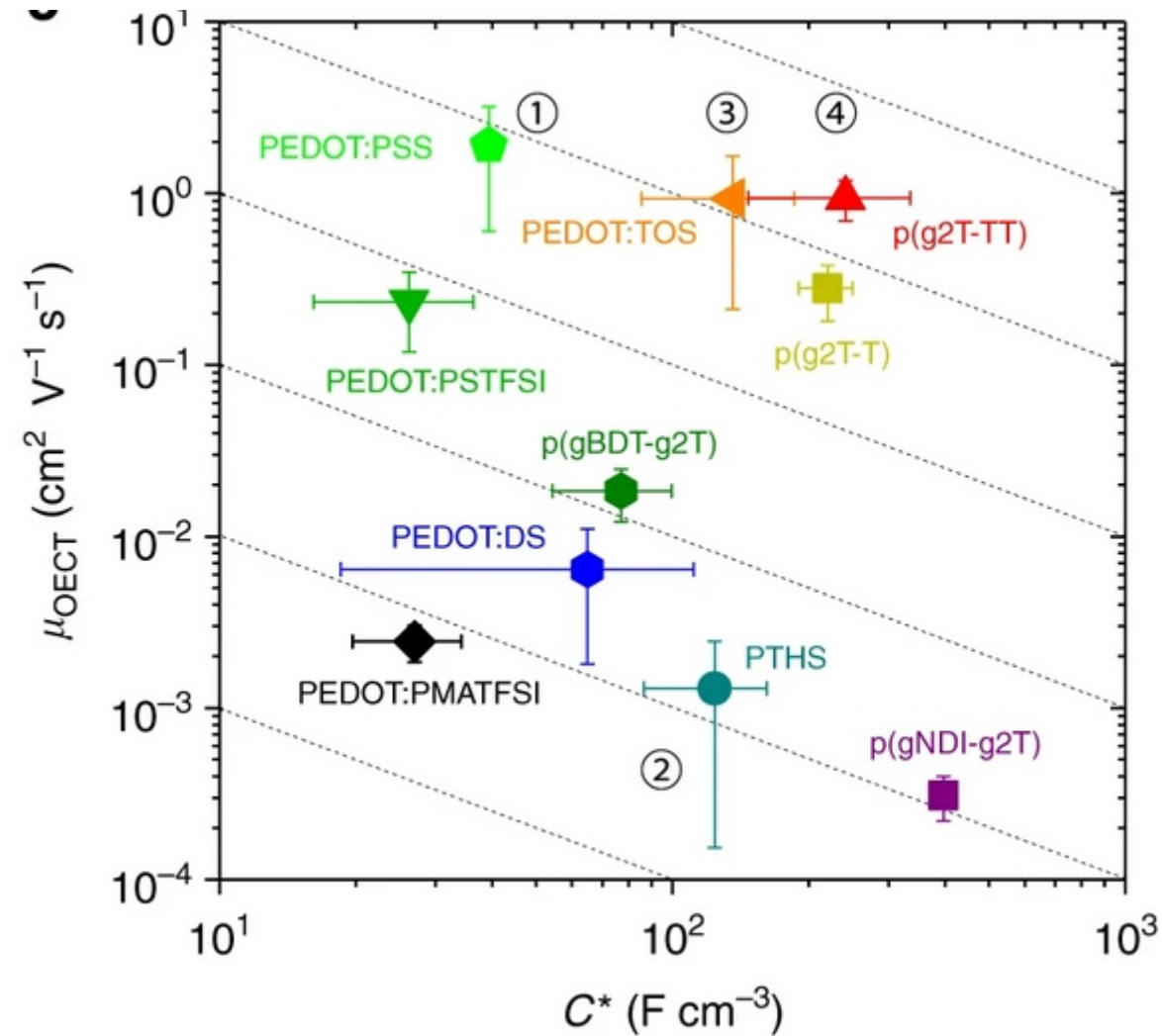
- μC^* Product
- Materials show comparably small difference in C^* (connected to swelling behavior)
- Same polymer backbone (e.g., PEDOT) can give very different mobility
→ swelling and transport are not directly linked to another!
- Measurements confirm that there is only a weak voltage dependence of μ and C^*



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4.4 Scaling of OECTs

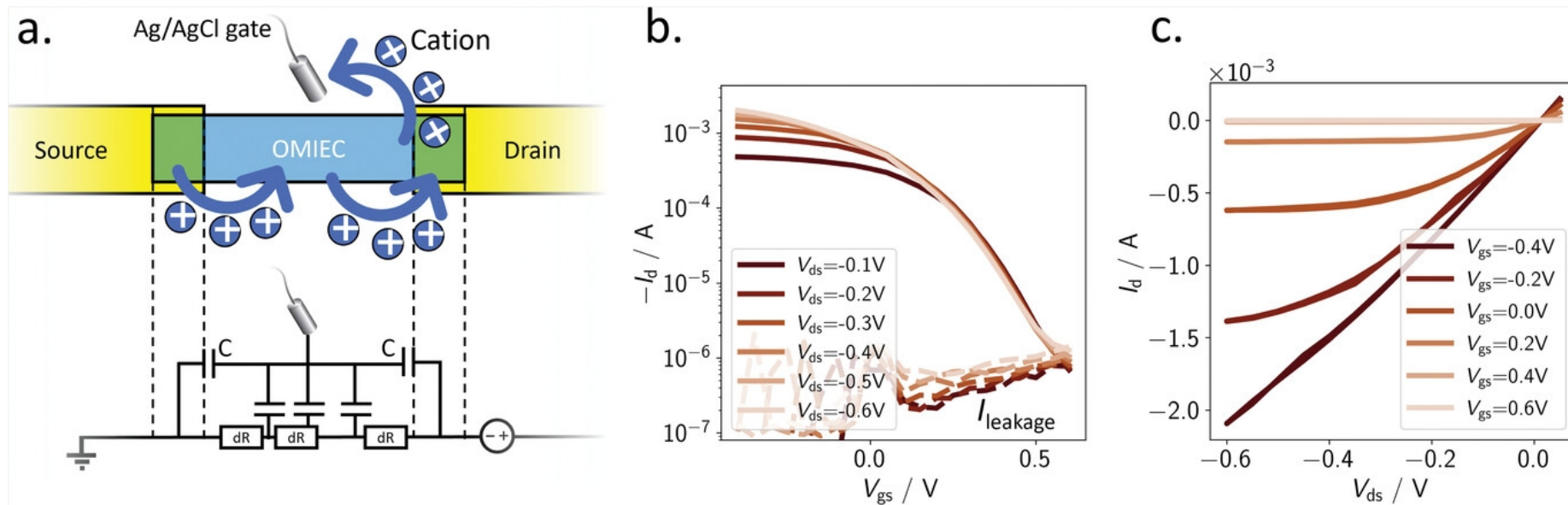
- μC^* Product
 - Be careful when measuring μC^*
 - Requires a Ag/AgCl gate/ a gate with infinite capacitance
 - Only true at $V_{DS} = 0V$ and very small OMIEC overlap at source and drain



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4.4 Scaling of OECTs

- **Scaling of ionic circuit**
 - The gate circuit is composed of at least two capacitors (gate and channel) and a resistor (electrolyte)
 - Ideally, C_G is infinite and for static switch the electrolyte resistance can be ignored
→ usually not the case in practise



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4.4 Scaling of OECTs

- **Gate capacitance scaling**

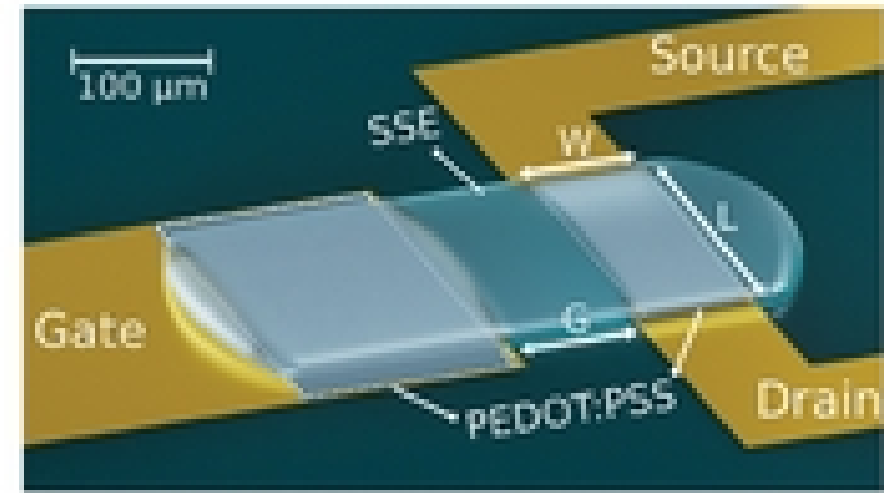
- Non polarizable gates or gates with infinite capacitance are ideal

→ DC voltage drop occurs only across the channel but

1) high gate capacitance requires large area electrodes ($A_{\text{gate}}:A_{\text{Channel}} >10:1$)

2) or Ag/AgCl electrode (usually not stable) (a)

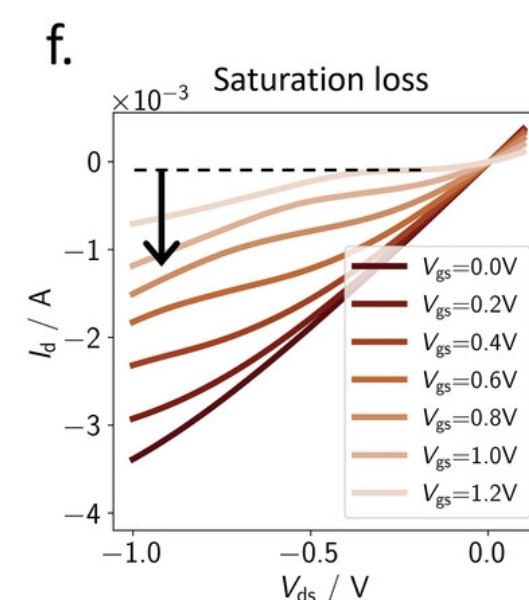
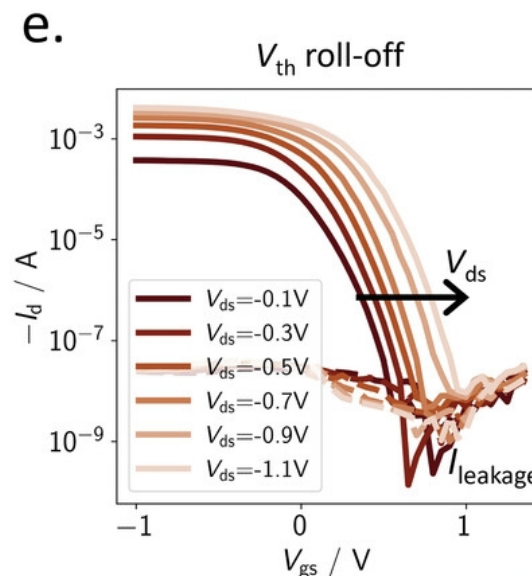
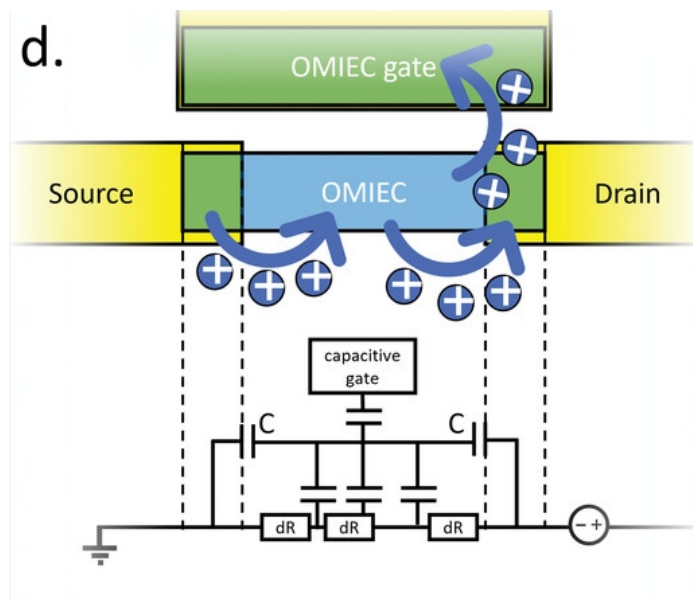
- Side-gate with OMIEC coating on gate electrode is the only way to obtain stable and scale performance
Gate usually covered with the same OMIEC to increase capacitance



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4.4 Scaling of OECTs

- **Gate capacitance scaling**
 - However, when integrating side-gates, also overlap capacitances need to be considered
 - Drain voltage (drain-OMIEC overlap) acts like a 2nd gate
 - For p-type: V_{DS} depletes channel at gate but increases doing a source (works against gate)
→ typical appearance of short-channel effects (loss of saturation and V_{th} roll-off)



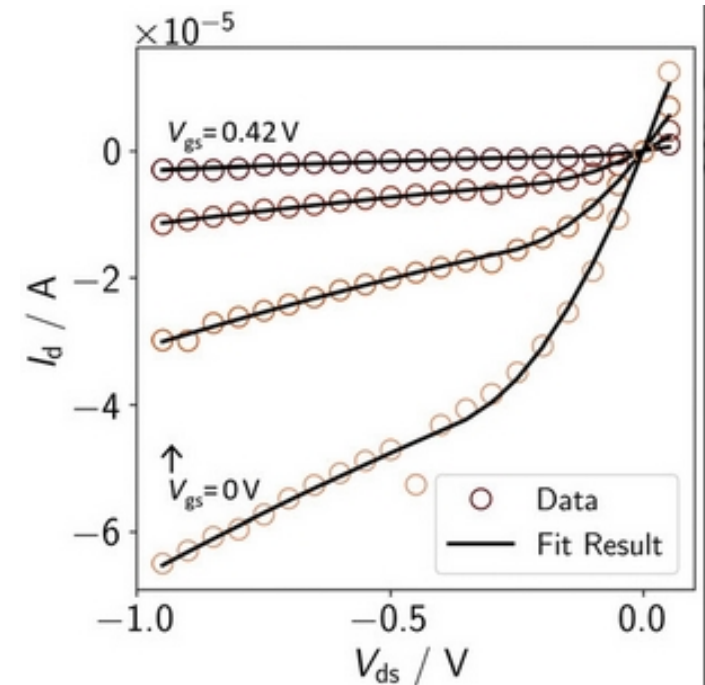
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4.4 Scaling of OECTs

- Gate capacitance scaling
- Drain effect can be modeled using charge-based model

$$I_{d,sat} = \frac{Wd\mu C^*}{2L} \left(\frac{C_g}{C_{total}} \left(V_{gs} - \frac{C_{total}}{C_g} V_t \right) + \frac{C_{ch} + 2C_d}{C_{total}} \frac{V_{ds}}{2} \right)^2$$

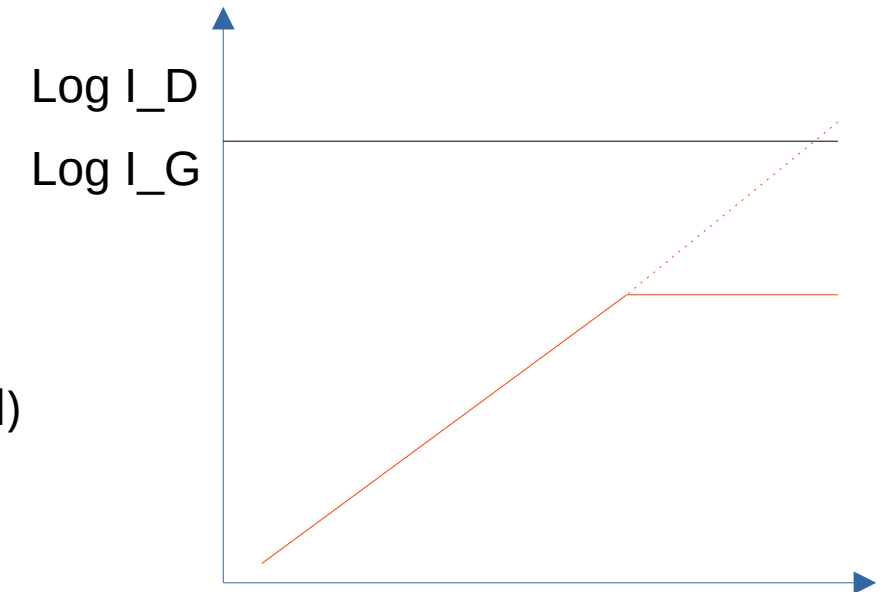
- Oversizing gate helps but not sufficient to minimize V_{th} roll-off and loss of saturation (Overlap has to go to zero, in practise $<5\mu\text{m}$!)



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4.4 Scaling of OECTs

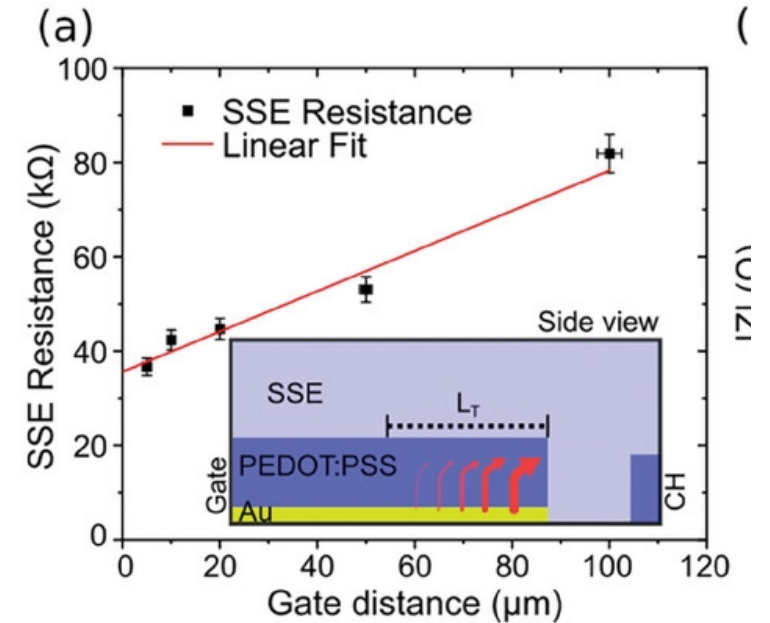
- **Including the ion conductivity**
 - Electrolyte resistance become dominant factor in AC operation
 - In OECTs always the electrolyte resistance rules/ determine the high-frequency cut-off
 - Usually the unity-gain cut-off frequency is not reached
 - Ionic conductivity is usually much smaller than electronic conductivity + channel length comparable to gate-channel distance (determine by patterning method)



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4.4 Scaling of OECTs

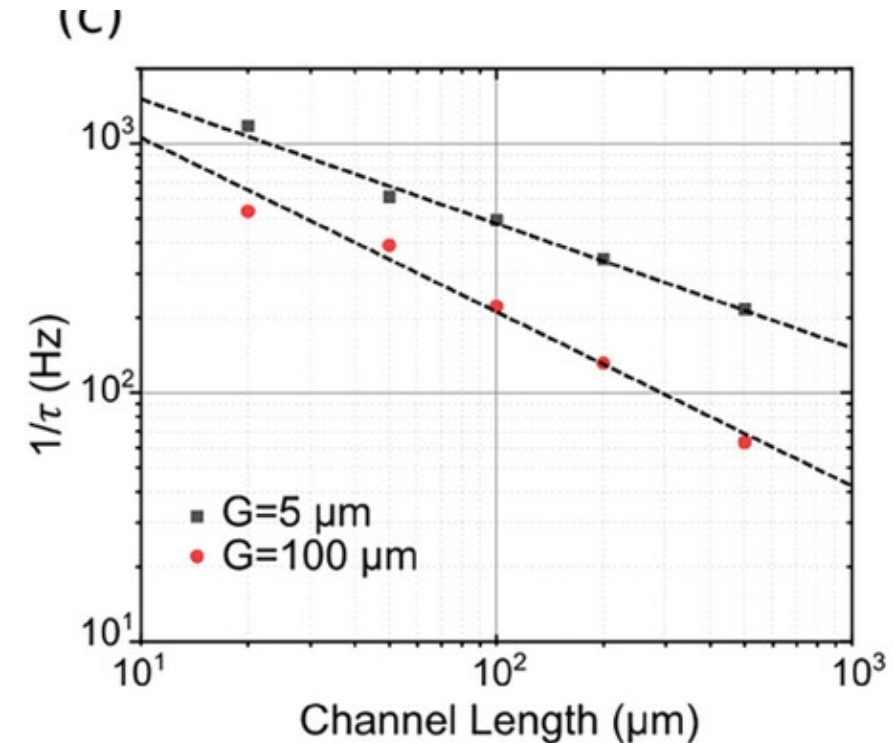
- **Including the ion conductivity**
 - Very low ion conductivity leads to current crowding effects (only small portion of the gate is active)
 - Even if gate distance goes to zero, resistance does not!
 - lower limit of resistance which can only be further reduce by reducing the channel area
 - L_T is the transfer length: minimum sheet resistance of electrolyte due to gate overlap



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4.4 Scaling of OECTs

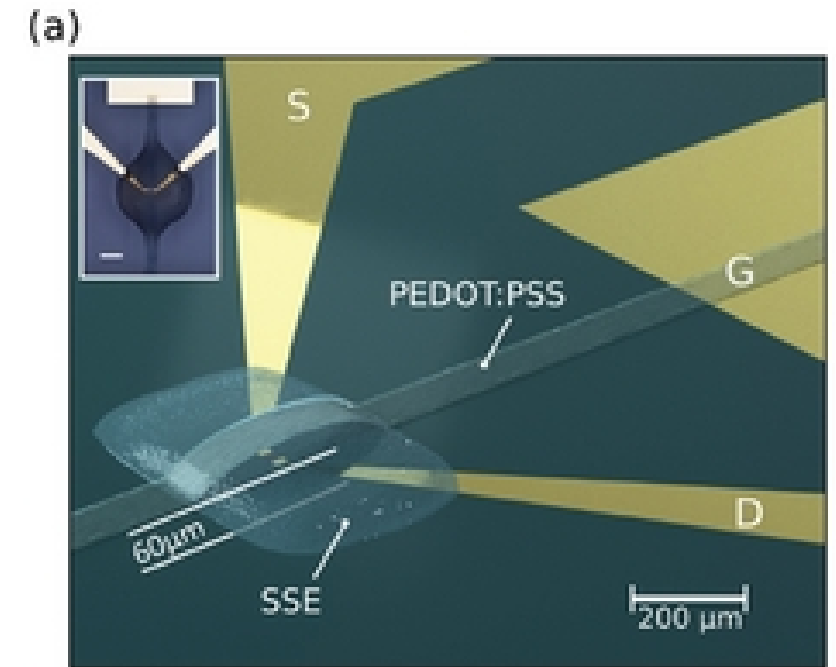
- **Including the ion conductivity**
 - Very low ion conductivity leads to current crowding effects (only small portion of the gate is active)
 - Even if gate distance goes to zero, resistance does not!
 - lower limit of resistance which can only be further reduce by reducing the channel area
 - gate delay time (RC) does not scale with channel length of gate distance as in MOSFETs ($f_t \sim 1/L^2$)



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4.4 Scaling of OECTs

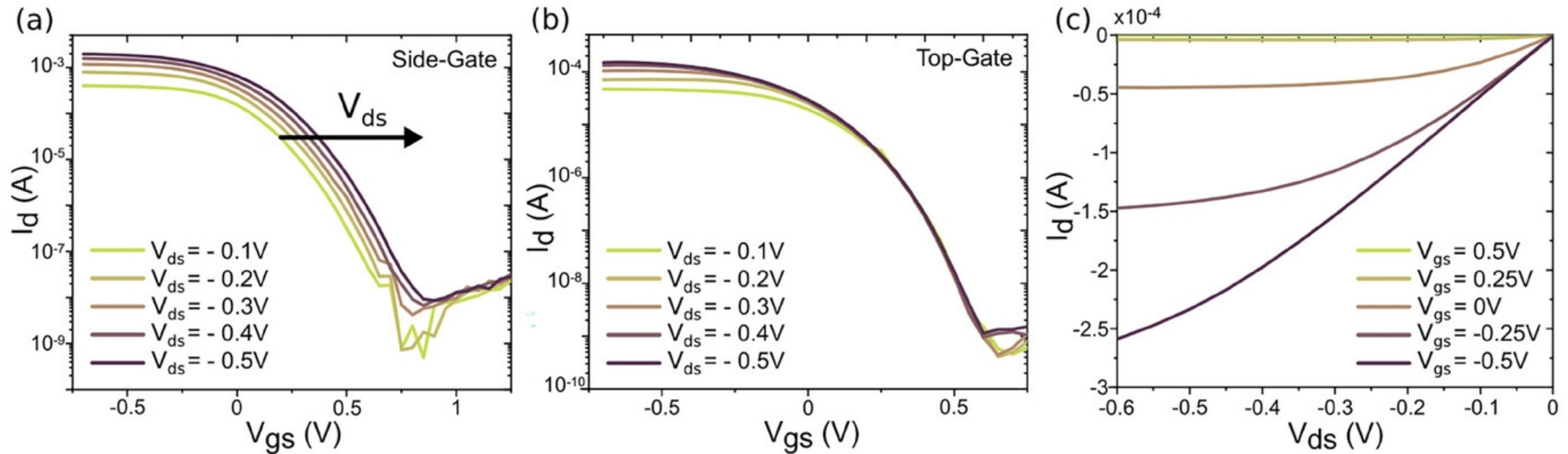
- **From side gate to top-gate**
 - Realistically the thickness of the electrolyte cannot be $<5\mu\text{m}$ (leaky, films dry up, different surface wetting)
 - Gate distance limited by lithography ($\sim 1\mu\text{m}$) but limiting factor is the transfer length L_T
 - Top-gate architecture:
 - Metallic Gate electrode / or PEDOT:PSS is printed onto electrolyte (minimal thickness required & viscosity)
 - Gate-to-Channel distance $\sim 30\mu\text{m}$ but capacitance of gate is fully utilized (no transfer length effect)



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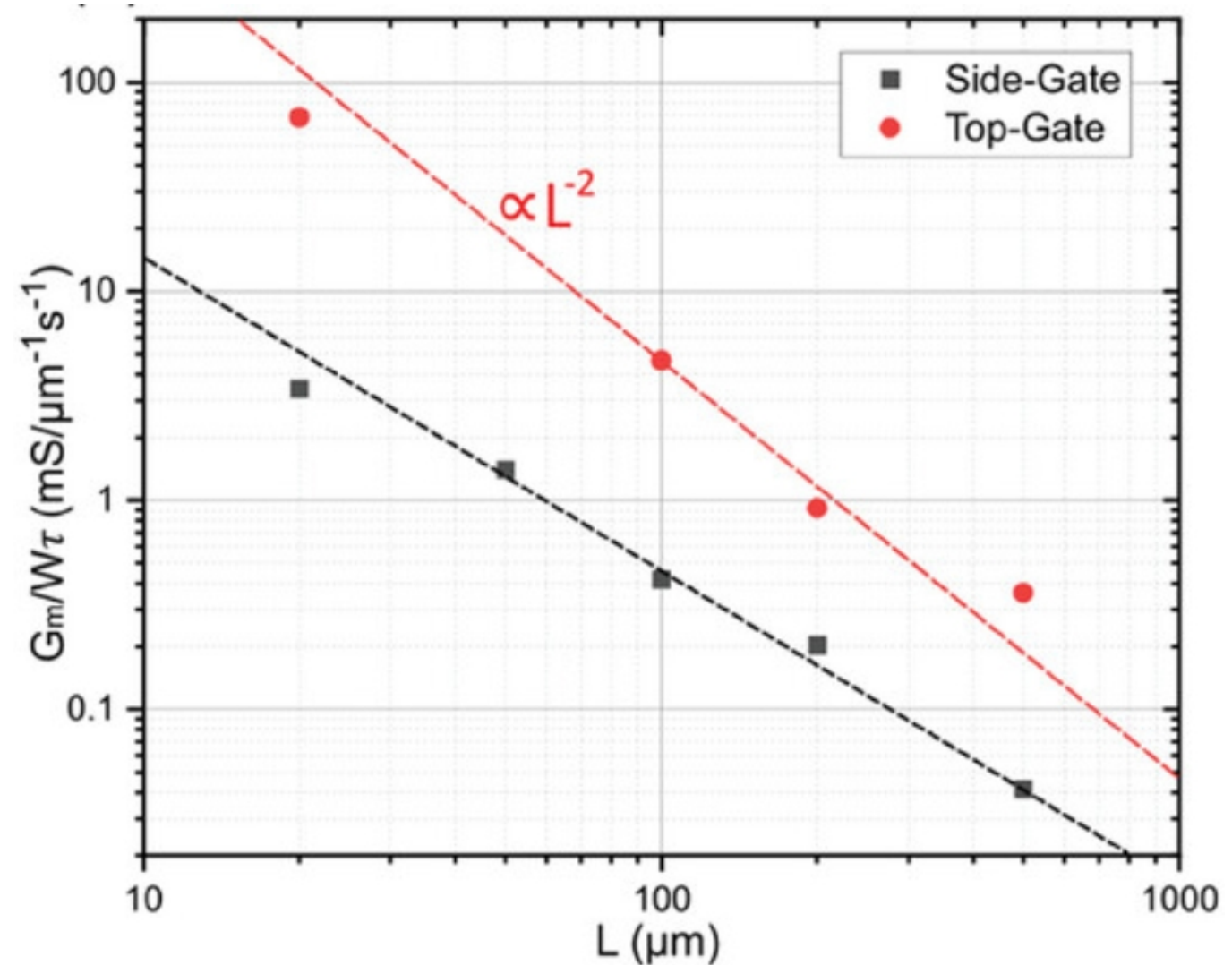
- From side gate to top-gate
- Top-Gate gives perfect saturation and no V_{th} roll-off



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4.4 Scaling of OECTs

- **From side gate to top-gate**
 - f_t of transistor scales with L^{-2} (ideal)
 - G_m/τ also scales with L^{-2}
 - G_m/τ as Figure of Merit ensures high gain (g_m) and high speed (τ)
 - If g_m/τ is high, the transistor uses its capacitance and transconductance most efficiently



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4.4 Scaling of OEECTs

- **How to design a fast and power efficient OEECT with high gain**
 - Use very thin OMIEC! Thickness brings gm up but on the cost of capacitance (slow)
 - Use OMIEC with very high mobility but not C! Brings up gain but not on the expense of speed of operation
 - Not every material can be cast into very thin-films (trade-off)
 - Ag/AgCl in Water gives always the best performance but devices cannot be integrated (only good for sensing)
 - Side-gate is easy to integration but overlap capacitance and electrolyte resistance lead to non-ideal scaling
 - Top-Gate benefits from effective usage of capacitance and gm
 - Ideal device would be a vertical channel, top-gate devices